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FORM PTO-1449 (Modified)		Attorney Docket No.: 12172-004530US		Application No.: 89/057,861	
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		Applicant: Howard G. Sachs		Group: 278	
		Filing Date: April 9, 1998		Page 1	
Reference Designation		U.S. PATENT DOCUMENTS			
Examiner Initial	Document No.	Date	Name	Class	Sub-class
FOREIGN PATENT DOCUMENTS					
	Document No.	Date	Country	Class	Sub-class
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)					
<u>✓✓</u> AA	Anderson, D.W. et al. [1967] "The IBM 360 model 91: Processor philosophy and instruction handling." IBM J. Research and Development 11:1 (January) pp 8-24.				
<u>✓✓</u> AB	Charlesworth, A.E., [1981]. "An approach to scientific processing: The architecture design of the AP-120B/FPS-164 family" Computer 14:9 (September), pp. 18-27.				
<u>✓✓</u> AC	Colwell, R.P. et al. [1987]. "A VLIW architecture for a trace scheduling compiler." Proc. second Conf. on Architectural Support for Programming Languages and Operating Systems, IEFF/ACM (March), pp. 180-192.				
<u>✓✓</u> AD	Dehnert, J.C. et al. [1989]. "Overlapped loop support on the Cydra 5." Proc. Third Conf. on Architectural Support for Programming Languages and Operating Systems (April), IEEE/ACM. Boston, pp. 26-39.				
<u>✓✓</u> AE	Rau, B.R., et al. [1989]. "The Cydra 5 departmental supercomputer: Design philosophies, decisions, and tradeoffs," IEEE Computers, 22:1 (January), pp. 12-34				
<u>✓✓</u> AF	Smith, J.E. [1989]. "Dynamic instruction scheduling and the astronautics ZS-I" Computer 22:7 (July), pp. 21-35				
<u>✓✓</u> AG	Smith, J.E. et al. [1987]. "The ZS-I central processors," Proc. Second Conf. on Architectural Support for Programming Languages and Operating Systems, IEEE/ACM (March), pp. 199-204.				
<u>✓✓</u> AH	Sohi, G.S. [1990], "Instruction issue logic for high-performance, interruptible, multiple functional unit pipelined computers," IEEE Trans. on Computers 39:3 (March), 349-359.				
<u>✓✓</u> AI	Sohi and Vajapeyam [1989]. "Tradeoffs in instruction format design for horizontal architectures," Proc. Second Conf. on Architectural Support for Programming Languages and Operating Systems, IEEE/ACM (April), pp. 15-25.				
<u>✓✓</u> AJ	Tomasulo, R.M. [1967], "An efficient algorithm for exploiting multiple arithmetic units," IBM J. Research and Development 11:1 (January), 25-33.				
<u>✓✓</u> AK	Weiss and Smith [1984]. "Instruction issue logic for pipelined supercomputers," Proc. 11th Symposium on Computer Architecture (June) pp. 110-118.				
EXAMINER <u>V. V</u> DATE CONSIDERED <u>1-29-01</u>					

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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Reference Designation		U.S. PATENT DOCUMENTS			Page 1
Examiner Initial	Document No.	Date	Name	Class	Sub-class
FOREIGN PATENT DOCUMENTS					
	Document No.	Date	Country	Class	Sub-class
✓✓ AA	0 496 928	08/05/92	EPO		
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)					
✓✓ AB	De Gloria et al., "A Programmable Instruction Format Extension to VLIW Architectures", <u>Proceedings: Computer Systems and Software Engineering</u> The Hague, May 4-8, 1992 pp:35-40				
✓✓ AC	Dorozhevets et al., "The El'brus-3 and MARS-M: Recent Advances In Russian High-Performance Computing", <u>The Journal of Supercomputing</u> 6(1):5-48 (1992)				
✓✓ AD	Kato et al., "Delayed Instruction Execution On A Long Instruction Word (LIW) Computer", <u>Systems and Computers in Japan</u> 23(14):13-22 (1992)				
EXAMINER	1/1. ✓✓		DATE CONSIDERED		1-29-01

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